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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/813,035 | 03/21/2001 | Masanari Asano | 024354-00001 | 2760 |

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| EXAMINER |
|---|
| WALLACE, SCOTT A |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2671 | |

DATE MAILED: 05/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/813,035 | ASANO, MASANARI | |
| | Examiner | Art Unit | |
| | Scott Wallace | 2671 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

***Response to Arguments***

1. Applicant's arguments filed 03/14/03 have been fully considered but they are not persuasive. In response to applicant's argument on page 6 last paragraph, "Knox simply does not teach that data are written in with the address of an additional area, and is particularly silent with respect to writing bitstreams, which are the actual data". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., data being written into the additional area being silent with respect to writing bitstreams) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The claim does disclose the data being written into the additional area being silent with respect to writing bitstreams. Knox discloses storing OSD data (other than image data) in a memory that is mapped into various buffers. One of the buffers is for OSD data (column 3 lines 5-10). This buffer is the additional area of the storage area.

2. In response to applicant's argument on page 7 last paragraph, "Sherburne fails to teach or suggest the operational relationship between the circuit components". Sherburne discloses "having described the general organization of the memory and memory data, and the circuitry for reading out and utilizing the same". There is a memory circuit and a circuit for reading out data from memory, therefore a relationship between the circuits. On page 8 the applicant claims that Sherburne does not teach an address generation circuit. An address circuit gives an address to store the data in memory. Sherburne discloses the memory is addressed with the image data (column 2 lines 17-21). Also, the applicant states that Sherburne's disclosure of the access control circuit and area adjustment circuit are based on improper reading of Sherburne. Sherburne discloses the circuitry for reading out of data from the memory (column 4 lines 51-55), which is what the access control circuitry does. The area adjustment circuit is part of the memory (column 2 lines 29-47).

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

1. Claims 12-15, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Knox et al.

2. As per claims 12 and 17, Knox et al discloses an image processing method comprising the steps of: setting up, in a storage circuit in which image data is stored, a range of an image area in which the image data is written and a range of an additional area which is adjacent to the image area and in which data other than the image data is written (column 3 lines 5-7), with information supplied to a memory space of said storage circuit as a parameter (column 3 lines 29-43); writing the data other than the image data from external into the additional area in said storage circuit according to a first write control signal(column 1 lines 50-53 and column 2 lines 48-55); writing the image data at an address location of the image area in said storage circuit according to a second write control signal (column 2 lines 48-55); and reading out the data stored in the additional area and the image data stored in the image area in said storage circuit in response to a first read control signal (column 4 lines 30-35).

3. As per claim 13, Knox et al discloses wherein said step of reading out the data comprises the steps of: reading out the data from the additional area in said storage circuit in response to the first read control signal (column 2 lines 48-55); and reading out the image data from the image area in said storage circuit in response to a second read control signal (column 2 lines 48-55).

4. As per claim 14, Knox et al discloses wherein the first write control signal and the read control signal are a transfer enable signal enabling an execution of processing (column 2 lines 48-65).

5. As per claim 15, Knox et al discloses wherein said step of reading out the data inserts the data read out from the additional area into a predetermined position of a video signal (column 4 lines 30-35).

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-2, 11 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherburne U.S. Patent No. 5,818,433 in view of Knierim U.S. Patent No. 4,755,810.

9. As per claims 1 and 16, Sherburne discloses an image processor comprising: a storage circuit storing therein image data (column 4 lines 24-40); a data input/output circuit controlling input/output of the image data (column 4 lines 52-55); an access control circuit controlling access of writing in and reading out the image data to and from said storage circuit (column 4 lines 52-55); a memory control circuit comprising an address generation circuit generating an address in said storage circuit to and from which the image data is written in and read out (column 2 lines 17-21), said memory control circuit comprising an area adjustment circuit which sets up an additional area adjacent to an area in which the image data is actually stored in a memory space of said storage circuit and storing therein data other than the image data (abstract and column 2 lines 29-47), which adjusts the address generated by said address generation circuit, and which reads out the image data from said storage circuit, including the data in the

additional area, in response to the address and a read control signal supplied to said storage circuit (column 2 lines 17-21). However, Sherburne does not disclose a refresh circuit controlling refreshing of said storage circuit. This is disclosed in Knierim in column 4 lines 24-35. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the refresh circuit of Knierim with the system of Sherburne because this would have kept the screen from flickering.

10. As per claim 2, Sherburne discloses wherein said area adjustment circuit sets up the additional area immediately preceding or following the area in which the image data is stored (column 2 lines 29-45).

11. As per claim 11, Sherburne discloses wherein said access control circuit supplies the data other than the image data to said memory circuit (column 4 lines 52-55).

12. Claims 3, 5-7, 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sherburne in view of Knierim in further in view of Knox et al., U.S. Patent No. 6,175,388.

13. As per claim 3, the combination of Sherburne and Knierim does not specifically disclose wherein information on a position of the additional area is supplied as setting information included in header information. However, this is disclosed in Knox et al in column 3 lines 39-55. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use this header information in Knox et al with the systems of Sherburne and Knierim because this allows the OSD bitstream to be modified by the user.

14. As per claims 5-7, the combination of Sherburne and Knierim does not specifically disclose wherein said area adjustment circuit obtains information on a base point in the memory space, a row direction width, and a column direction width and outputs the obtained information to said address generation circuit as a parameter. However, this is disclosed in Knox et al in column 3 lines 29-43. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use this information of Knox et al with the systems of Sherburne and Knierim because this allows the memory for the other data to be adjustable.

15. As per claims 8-10, Knox et al discloses wherein said area adjustment circuit supplies the data, which is read out from the additional area, to a predetermined positional in a video signal (column 32-37).

16. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sherburne in view of Knierim in further in view of Herz et al., U.S. Patent No. 5,883,675.

17. As per claim 4, The systems of Sherburne and Knierim do not specifically disclose wherein said area adjustment circuit sets a size of the additional area using information, which is obtained in synchronization with a supplied vertical synchronization signal, as a parameter and reads out the data stored in the additional area in response to a data transfer request. However, this is disclosed in Herz et al in column 1 lines 13-15. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the vertical synchronization signal in Herz with the systems of Sherburne and Knierim because this is the part where no video data is being sent so other types of data have a chance to be sent.

***Conclusion***

**18. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action

is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Scott Wallace** whose telephone number is **703-605-5163**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Mark Zimmerman**, can be reached at 703-305-9798.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

MARK ZIMMERMAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600